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CLAIMS

1. A method for detecting process variations, the method comprising the steps of:
controlling count gate control by a first circuit;
generating at least one clock count by a second circuit; and
outputting results of the clock count by a third circuit.
2. The method of claim 1, wherein the step of controlling comprises the steps of:
activating a scan signal;
toggling a clock signal; and
setting a reset signal on.
3. The method of claim 2, wherein the step of controlling further comprises the steps of:
selecting an oscillator by activating and toggling the signals;
enabling the oscillator; and
setting the reset signal off.
4. The method of claim 2, wherein the step of controlling further comprises the step of
toggling the clock signal for a period of time.
5. The method of claim 1, wherein the step of generating further comprises the steps of:
outputting the count into a counter; and
reading the count into a scan chain.
6. The method of claim 4, wherein the step of toggling further comprises the step of
storing the output of the toggle in a counter.

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3 7. The method of claim 5, further comprises the step of toggling the clock for reading out
4 the clock count.

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6 8. The method of claim 1, further comprising the step of communicating with a JTAG
7 interface.

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9 9. The method of claim 4, further comprises the step of communicating with a JTAG
10 interface.

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12 10. An apparatus to detect process variations comprising:
13 a first circuit to select a clock;
14 a second circuit connected to the first circuit to generate at least one clock count; and
15 a third circuit connected to the first circuit to output a result of the clock count.

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17 11. The apparatus of claim 10, wherein the first circuit comprises:
18 a scan signal; and
19 a clock signal, wherein the scan signal and the clock signal turn on at least one clock.

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21 12. The apparatus of claim 11, wherein the first circuit further comprises:
22 a reset signal; and
23 an enable signal, wherein the enable signal enables the at least one clock.

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25 13. The apparatus of claim 11, wherein the clock signal is toggled for a period of time.

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27 14. The apparatus of claim 13, wherein the second circuit further comprises outputting a
28 count of the toggle.

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3 15. The apparatus of claim 14, wherein the third circuit comprises:

4 a counter; and

5 a scan chain, wherein the scan chain is connected to the counter.

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7 16. The apparatus of claim 15, wherein the count is input to the counter.

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9 17. The apparatus of claim 15, wherein the reset signal is input to the counter.

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11 18. The apparatus of claim 16, wherein the scan chain further comprises a read signal,

12 wherein the read signal reads the count into the scan chain.

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14 19. The apparatus of claim 18, wherein the clock signal is toggled to read out the count

15 from the scan chain.

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17 20. The apparatus of claim 10, wherein communicates with a JTAG interface.

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